# 8051 Tutorials

- www.8052.com\tut8051.html
- www.mikroelektronika.co.yu\english\product\books\8051book\00.htm


# MCS-51 Periféricos incluidos: Interfaz Serie

(MSB) (LSB)

| SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI |
|---|---|---|---|---|---|---|---|

Where SM0, SM1 specify the serial port mode, as follows:

| SM0 | SM1 | Mode | Description | Baud Rate |
|---|---|---|---|---|
| 0 | 0 | 0 | shift register | $f_{osc}/12$ |
| 0 | 1 | 1 | 8-bit UART | variable |
| 1 | 0 | 2 | 9-bit UART | $f_{osc}/64$ or $f_{osc}/32$ |
| 1 | 1 | 3 | 9-bit UART | variable |

- SM2 enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1 then RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be 0.
- REN enables serial reception. Set by software to enable reception. Clear by software to disable reception.
- TB8 is the 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
- RB8 in Modes 2 and 3, is the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
- TI is transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
- RI is receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

**SCON: Serial Port Control Register**

$$\text{Mode 0 Baud Rate} = \frac{\text{Oscillator Frequency}}{12}$$

$$\text{Mode 2 Baud Rate} = \frac{2^{SMOD}}{64} \times (\text{Oscillator Frequency})$$

$$\text{Modes 1, 3 Baud Rate} = \frac{2^{SMOD}}{32} \times (\text{Timer 1 Overflow Rate})$$

# MCS-51 Periféricos incluidos: Interfaz Serie

Uso del Timer 1 como generador de *Baud Rate*

$$\text{Modes 1, 3 Baud Rate} = \frac{2^{SMOD}}{32} \times (\text{Timer 1 Overflow Rate})$$

Si modo timer auto-reload:

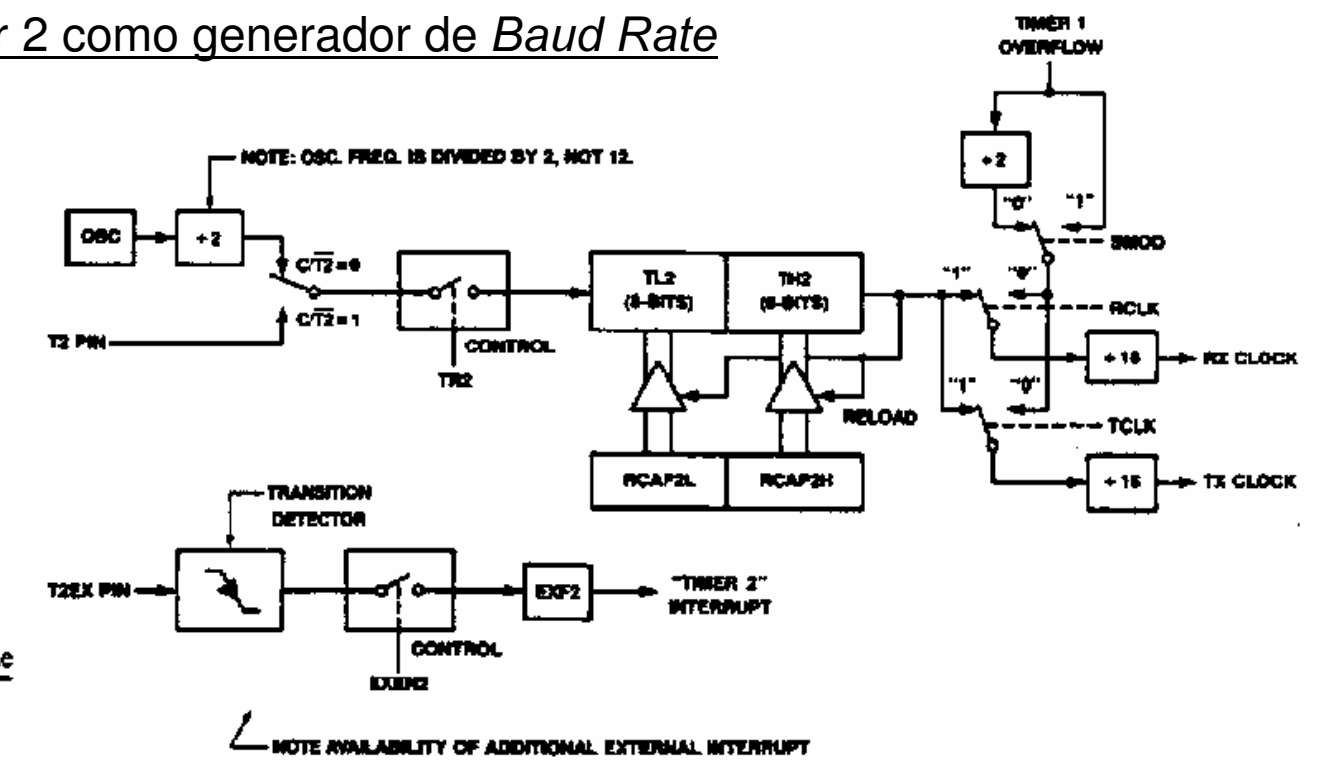
$$\text{Modes 1, 3 Baud Rate} = \frac{2^{SMOD}}{32} \times \frac{\text{Oscillator Frequency}}{12x\,[256 - (TH1)]}$$

| Baud Rate | $f_{osc}$ | SMOD | Timer 1 | | |
|---|---|---|---|---|---|
| | | | C/$\overline{T}$ | Mode | Reload Value |
| Mode 0 Max: 1 MHZ | 12 MHZ | X | X | X | X |
| Mode 2 Max: 375K | 12 MHZ | 1 | X | X | X |
| Modes 1, 3: 62.5K | 12 MHZ | 1 | 0 | 2 | FFH |
| 19.2K | 11.059 MHZ | 1 | 0 | 2 | FDH |
| 9.6K | 11.059 MHZ | 0 | 0 | 2 | FDH |
| 4.8K | 11.059 MHZ | 0 | 0 | 2 | FAH |
| 2.4K | 11.059 MHZ | 0 | 0 | 2 | F4H |
| 1.2K | 11.059 MHZ | 0 | 0 | 2 | E8H |
| 137.5 | 11.986 MHZ | 0 | 0 | 2 | 1DH |
| 110 | 6 MHZ | 0 | 0 | 2 | 72H |
| 110 | 12 MHZ | 0 | 0 | 1 | FEEBH |

**Figure 15. Timer 1 Generated Commonly Used Baud Rates**

# MCS-51 Periféricos incluidos: Interfaz Serie

Uso del Timer 2 como generador de *Baud Rate*




**Timer 2 in Baud Rate Generator Mode**

$$\text{Modes 1, 3 Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

Si modo timer (%2):

$$\text{Modes 1, 3 Baud Rate} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H, RCAP2L})]}$$

# MCS-51 I. Serie

## Modo 0

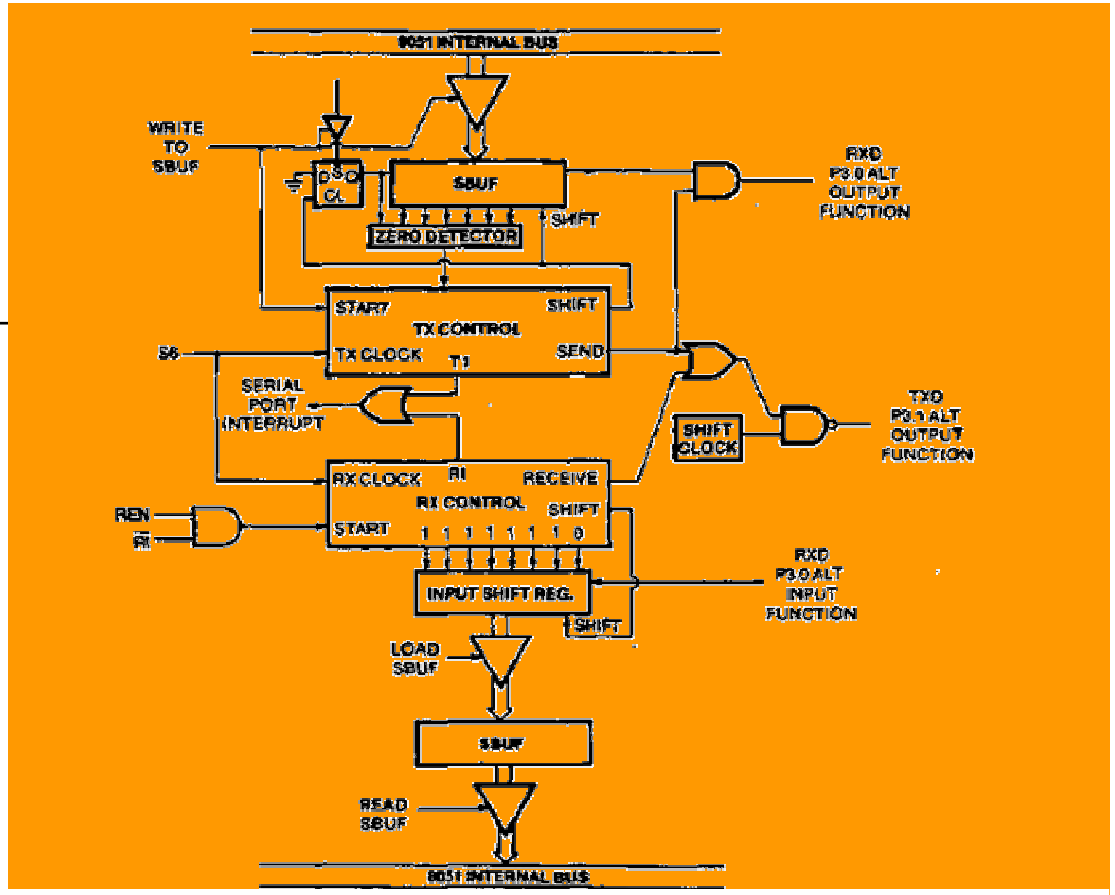



**FIGURE 2.14** Shift Register Mode 0 Timing

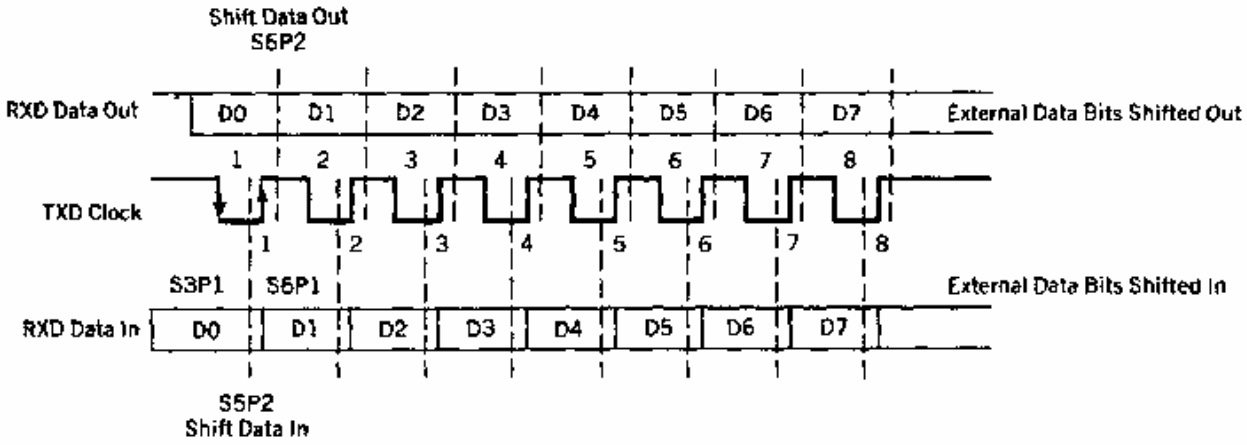



Figure 17. Serial Port Mode 0

# MCS-51 I. Serie

Modo 1

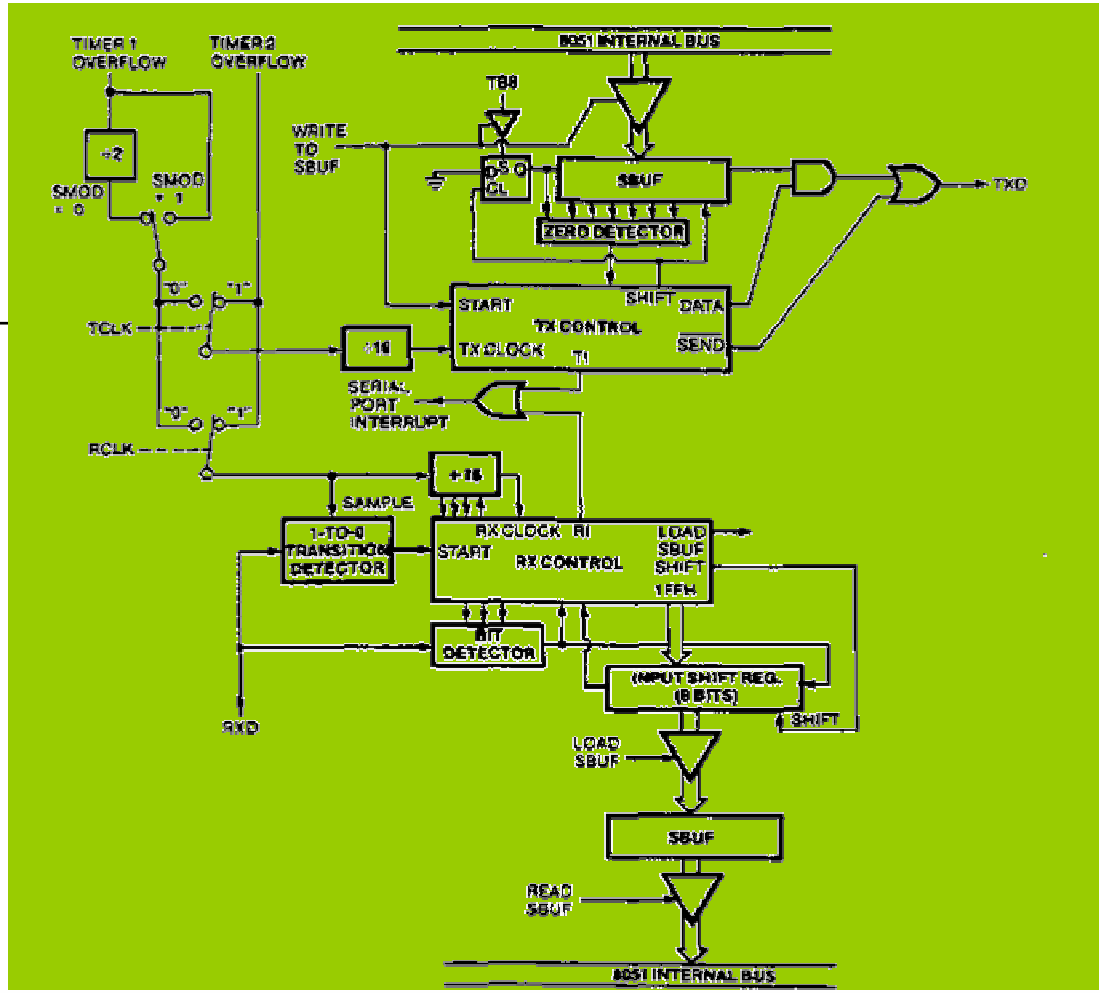



**FIGURE 2.15** Standard UART Data Word

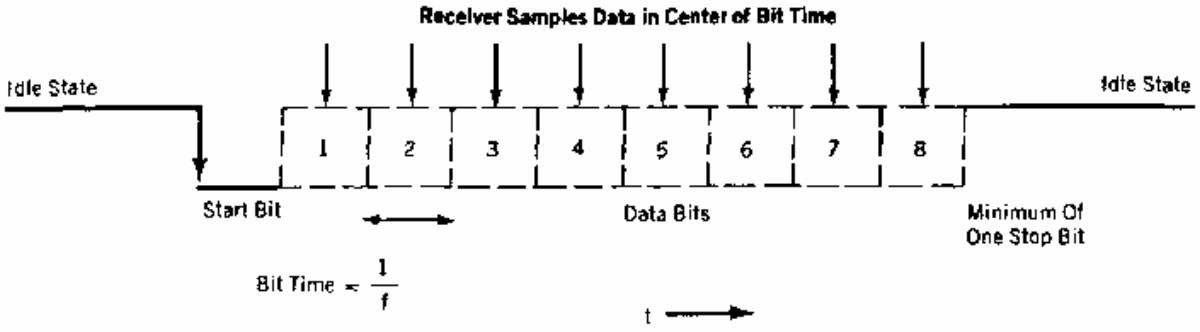
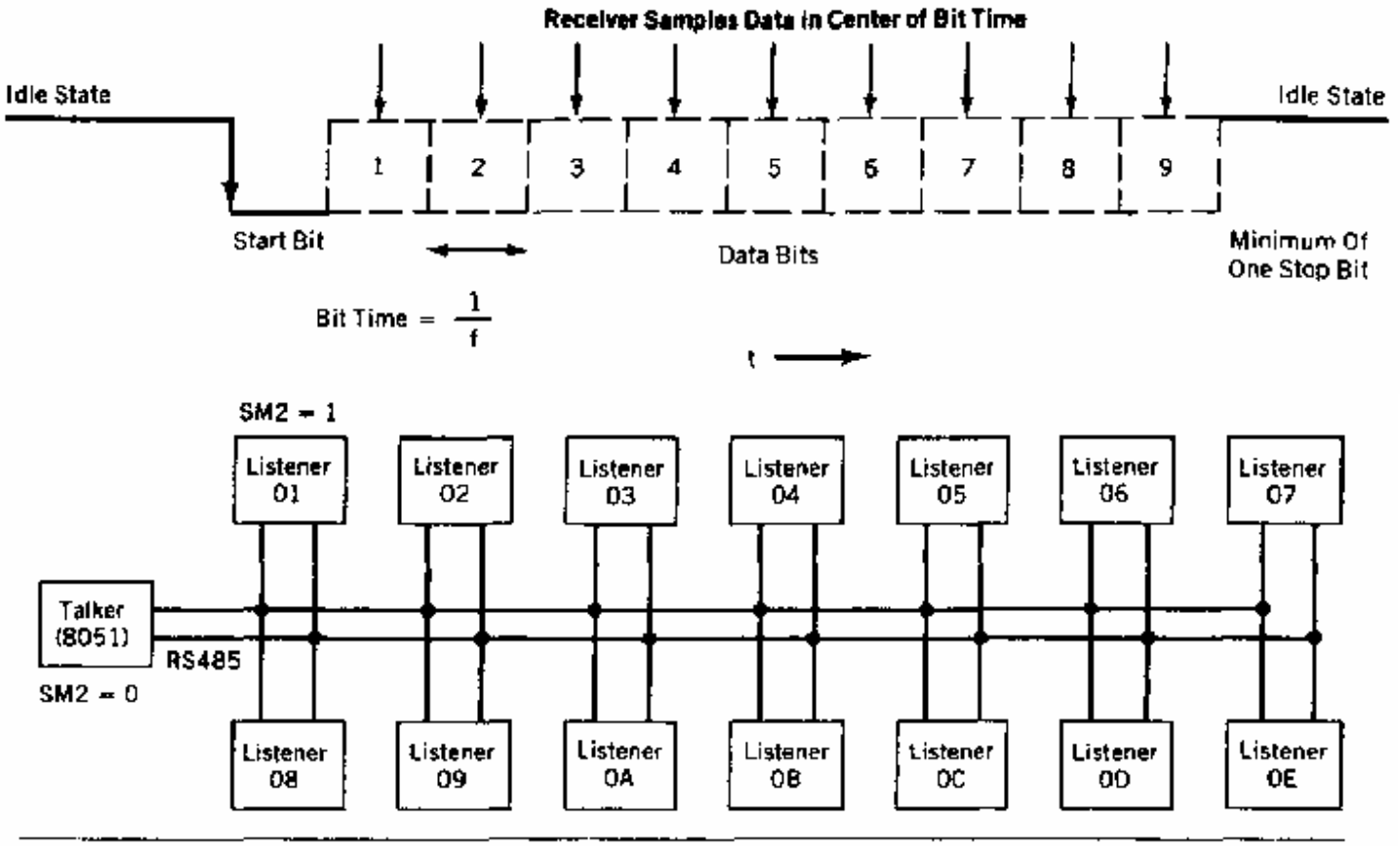



**Figure 18. Serial Port Mode 1. TCLK, RCLK and Timer 2 are Present in the 8052/8032 Only.**

# MCS-51 I. Serie

Comunicación multiprocesador

**FIGURE 2.16** Multiprocessor Data Word



# MCS-51 Power Save mode (CHMOS)

- Idle
- Power down

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| SMOD | - | - | - | GF1 | GF0 | PD | IDL |

| Symbol | Position | Name and Function |
|---|---|---|
| SMOD | PCON.7 | Double Baud rate bit. When set to a 1 and Timer 1 is used to generate baud rate, and the Serial Port is used in modes 1, 2, or 3. |
| — | PCON.6 | (Reserved) |
| — | PCON.5 | (Reserved) |
| — | PCON.4 | (Reserved) |
| GF1 | PCON.3 | General-purpose flag bit. |
| GF0 | PCON.2 | General-purpose flag bit. |
| PD | PCON.1 | Power Down bit. Setting this bit activates power down operation. |
| IDL | PCON.0 | Idle mode bit. Setting this bit activates idle mode operation. |

If 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XXX0000).
In the HMOS devices the PCON register only contains SMOD. The other four bits are implemented only in the CHMOS devices. User software should never write 1s to unimplemented bits, since they may be used in future MCS-51 products.

**Figure 28. PCON: Power Control Register**

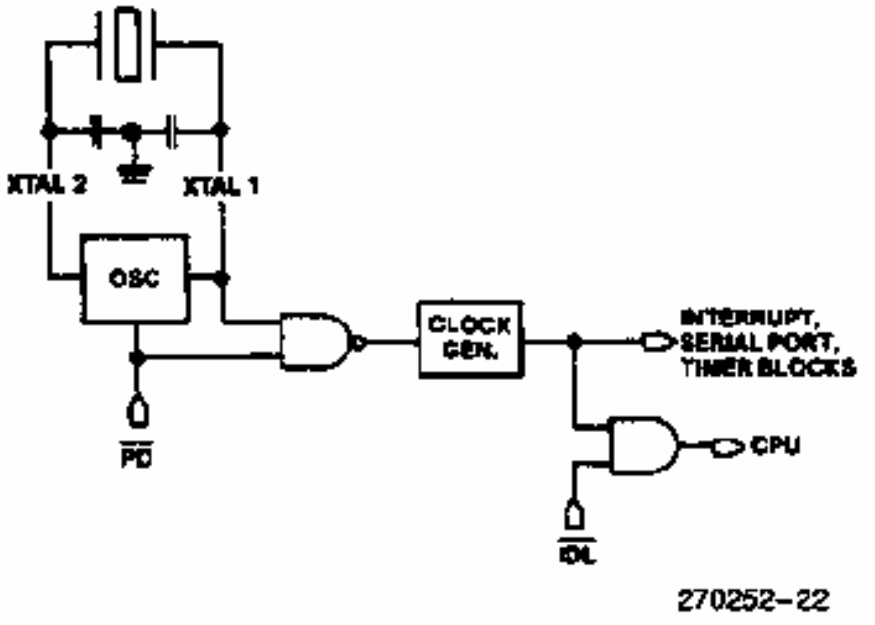



**Figure 27. Idle and Power Down Hardware**

# MCS-51 Versiones con EPROM

Table 4. EPROM Versions of the 8051 and 8052

| Device Name | EPROM Version | EPROM Bytes | Ckt Type | VPP | Time Required to Program Entire Array |
|---|---|---|---|---|---|
| 8051AH | 8751H/8751BH | 4K | HMOS | 21.0V/12.75V | 4 minutes |
| 80C51BH | 87C51 | 4K | CHMOS | 12.75V | 13 seconds |
| 8052AH | 8752BH | 8K | HMOS | 12.75V | 26 seconds |

Seguridad contra piratería:

- Lock bit en 8751H

- Array de encriptado y Lock bit en 8751BH, 8752BH y 87C51

Table 6. Program Protection

| Device | Lock Bits | Encrypt Array |
|---|---|---|
| 8751BH | LB1, LB2 | 32 Bytes |
| 8752BH | LB1, LB2 | 32 Bytes |
| 87C51 | LB1, LB2, LB3 | 64 Bytes |

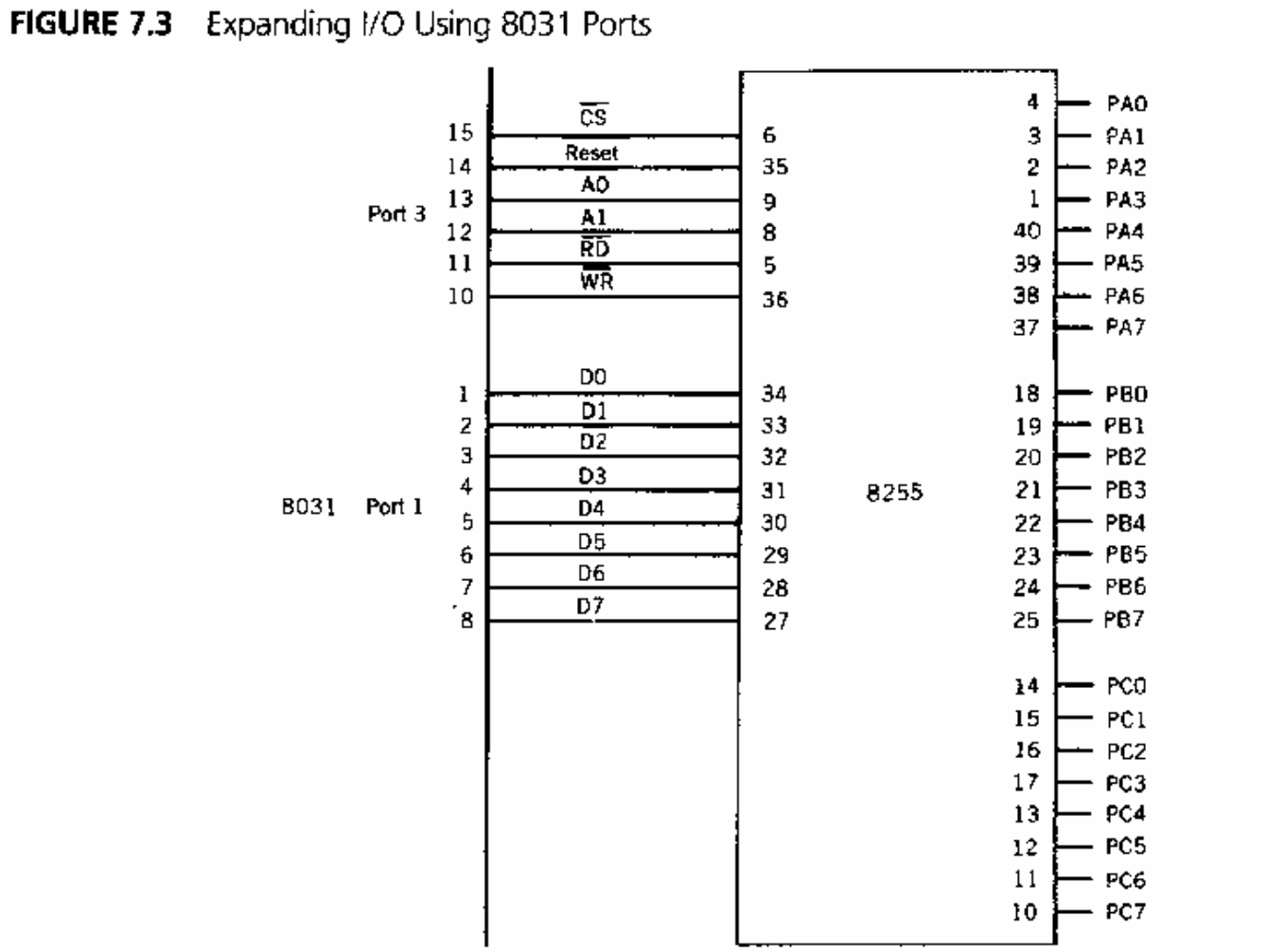
| Program Lock Bits | | | | Protection Type |
|---|---|---|---|---|
| | LB1 | LB2 | LB3 | |
| 1 | U | U | U | No program lock features enabled. (Code verify will still be encrypted by the encryption array if programmed.) |
| 2 | P | U | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled. |
| 3 | P | P | U | Same as 2, also verify is disabled. |
| 4 | P | P | P | Same as 3, also external execution is disabled. |

P-Programmed
U-Unprogrammed

Any other combination of the Lock Bits is not defined.

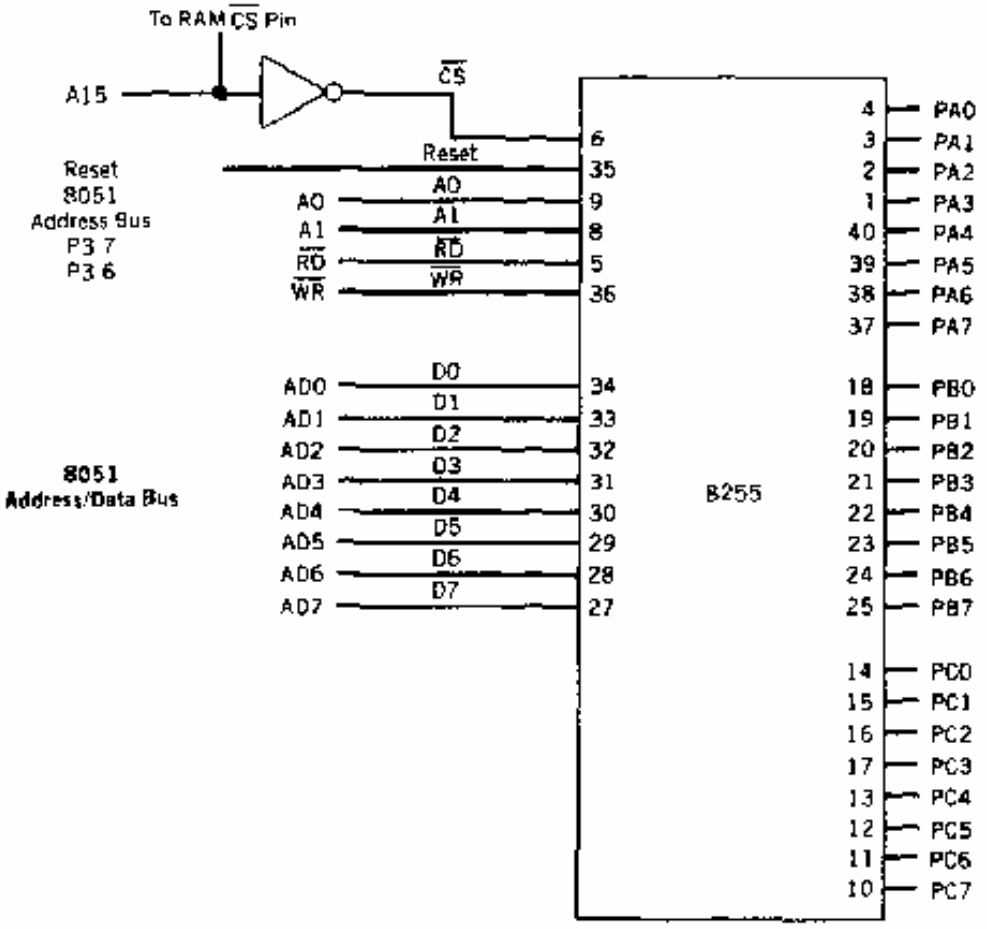
# MCS-51 Expansión de Puertos

**FIGURE 7.3** Expanding I/O Using 8031 Ports



# MCS-51 Expansión de Puertos

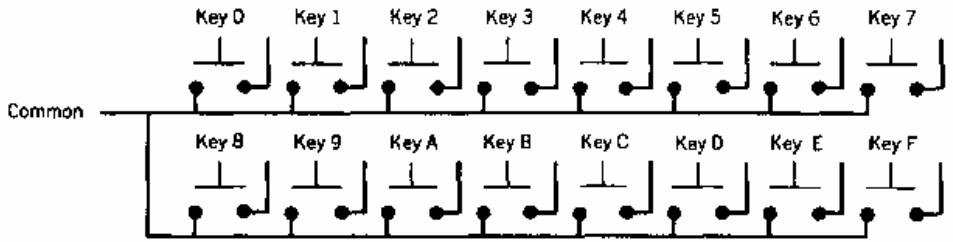
**FIGURE 7.4** Expanding I/O Using Memory Mapping



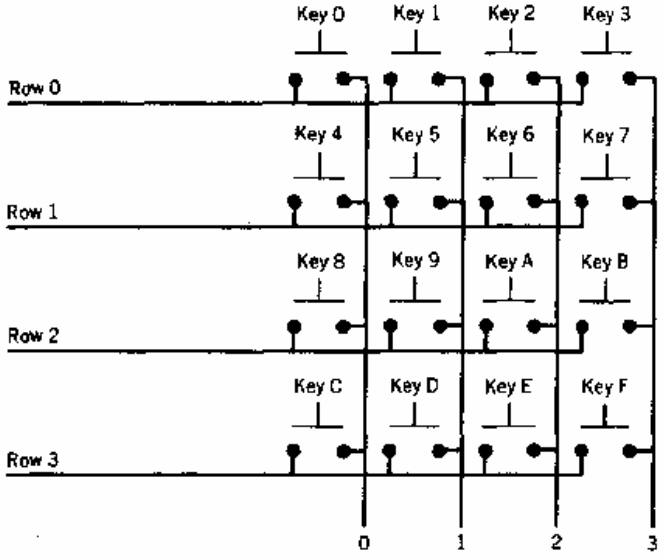

8255 Connections For Memory Mapping

# Detección de pulsadores

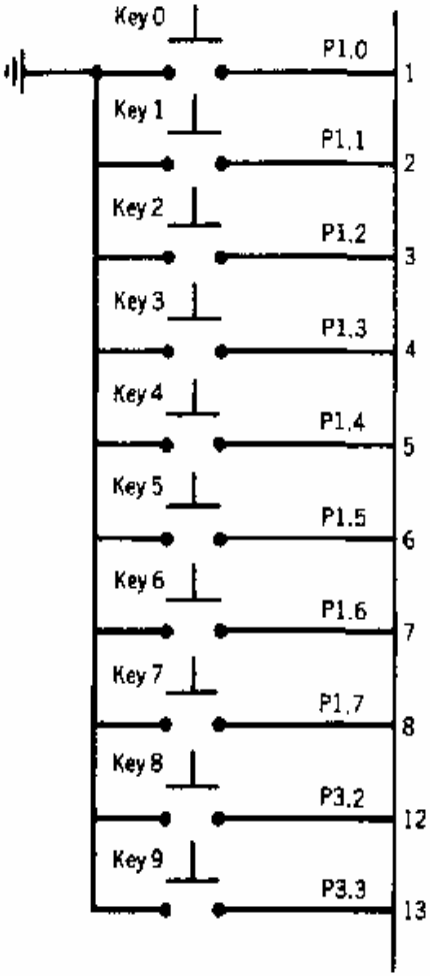
**FIGURE 8.1** Hypothetical Keyboard Wiring Configurations




(a) Lead-Per-Key Keyboard

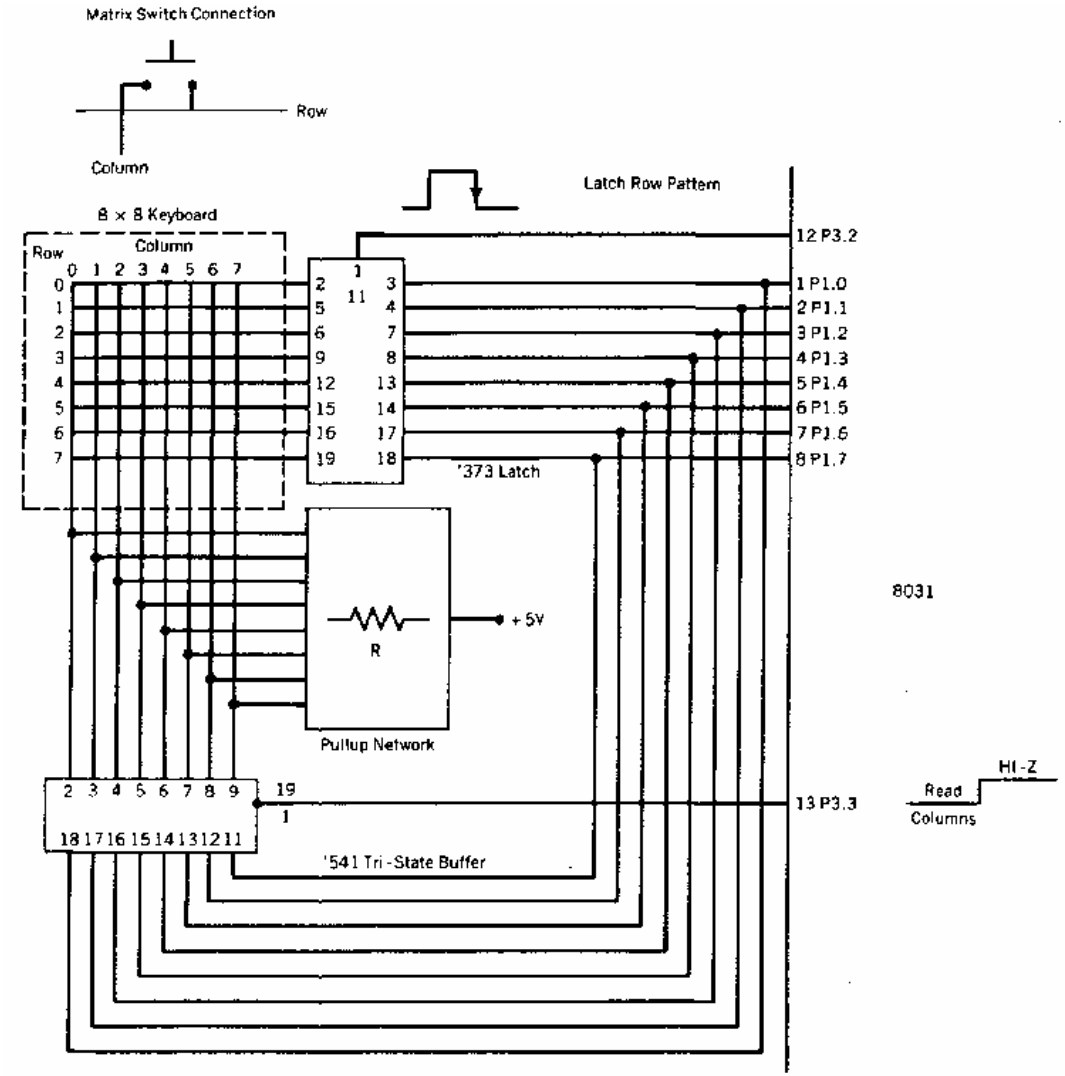



(b) X-Y Matrix Keyboard




8031

# Detección de teclas



# Conexión de leds

**FIGURE 8.7** Seven-Segment Display Circuit Used for "Svnseg" Program